# CLAIMS

**I Claim:**

1. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly;

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat; and

a conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts and electrically connects the leads;

wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

2. The stacked device of claim 1, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

3. The stacked device of claim 1, wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.

4. The stacked device of claim 1, wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

5. The stacked device of claim 1, wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

6. The stacked device of claim 5, wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

7. The stacked device of claim 1, wherein the conductive bond is spaced from the insulative housings.

8. The stacked device of claim 1, wherein the conductive bond is outside the peripheries of the insulative housings.

9. The stacked device of claim 1, wherein the conductive bond has a substantially spherical shape.

10. The stacked device of claim 1, wherein the stacked device is devoid of wire bonds and TAB leads.

11. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly, extends laterally from the first peripheral side surface a first distance, and extends downwardly beyond the first bottom surface;

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat, extends laterally from the second peripheral side surface a second distance, and does not extend downwardly beyond the second bottom surface; and

a conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts and electrically connects the leads;

wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the leads do not contact any insulative

material of the stacked device outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, and the first distance is greater than the second distance.

12. The stacked device of claim 11, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

13. The stacked device of claim 11, wherein the insulative housings are essentially identical to and vertically aligned with one another.

14. The stacked device of claim 11, wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

15. The stacked device of claim 11, wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

16. The stacked device of claim 15, wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

17. The stacked device of claim 11, wherein the conductive bond is spaced from the insulative housings and outside the peripheries of the insulative housings.

18. The stacked device of claim 11, wherein the conductive bond contacts only the leads.

19. The stacked device of claim 11, wherein the conductive bond has a substantially spherical shape.

20. The stacked device of claim 11, wherein the stacked device is devoid of wire bonds and TAB leads.

21. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces, wherein the first bottom surface includes a first peripheral ledge and a first central portion that is within and recessed relative to and non-integral with the first peripheral ledge;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly, extends laterally from the first peripheral side surface at the first peripheral ledge, and extends downwardly beyond the first bottom surface at the first peripheral ledge;

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces, wherein the second bottom surface includes a second peripheral ledge and a second central portion that is within and recessed relative to and non-integral with the second peripheral ledge;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat, extends laterally from the second peripheral side

surface at the second peripheral ledge, and does not extend downwardly beyond the second bottom surface at the second peripheral ledge; and

a conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device and contacts and electrically connects the leads;

wherein the insulative housings are essentially identical to and vertically aligned with one another, the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

22. The stacked device of claim 21, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

23. The stacked device of claim 21, wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

24. The stacked device of claim 21, wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

25. The stacked device of claim 21, wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

26. The stacked device of claim 25, wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

27. The stacked device of claim 21, wherein the conductive bond is spaced from the insulative housings and outside the peripheries of the insulative housings.

28. The stacked device of claim 21, wherein the conductive bond contacts only the leads.

29. The stacked device of claim 21, wherein the conductive bond has a substantially spherical shape.

30. The stacked device of claim 21, wherein the stacked device is devoid of wire bonds and TAB leads.

31. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a first distal end;

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat and extends laterally between the second peripheral side surface and a second distal end; and

a conductive bond outside the insulative housings and outside the peripheries of the insulative housings that extends laterally beyond any insulative material of the stacked device, contacts and electrically connects the leads and does not contact any other material;

wherein the insulative housings are essentially identical to and vertically aligned with one another, the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

32. The stacked device of claim 31, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

33. The stacked device of claim 31, wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

34. The stacked device of claim 31, wherein the second corner laterally extends a first distance from the first peripheral side surface, the second distal end laterally extends a second distance from the second peripheral side surface, and the first distance is greater than the second distance.

35. The stacked device of claim 31, wherein the first corner laterally extends a first distance from the first peripheral side surface, the second distal end laterally extends a second distance from the second peripheral side surface, and the first and second distances are essentially identical.

36. The stacked device of claim 31, wherein the conductive bond is laterally aligned with the second bottom surface.

37. The stacked device of claim 31, wherein the conductive bond is closer to the second bottom surface than to the first bottom surface.

38. The stacked device of claim 31, wherein the conductive bond contacts only the inner lateral portion and the second lead.

39. The stacked device of claim 31, wherein the conductive bond has a substantially spherical shape.

40. The stacked device of claim 31, wherein the stacked device is devoid of wire bonds and TAB leads.

41. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly and extends downwardly beyond the first bottom surface;

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat; and

a conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device, does not overlap any insulative material of the stacked device, is not overlapped by any insulative material of the stacked device and contacts and electrically connects the leads;

wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

42. The stacked device of claim 41, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

43. The stacked device of claim 41, wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

44. The stacked device of claim 41, wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

45. The stacked device of claim 44, wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

46. The stacked device of claim 41, wherein the conductive bond is laterally aligned with the second bottom surface, and is not laterally aligned with the first bottom surface.

47. The stacked device of claim 41, wherein the conductive bond does not contact any insulative material of the stacked device.

48. The stacked device of claim 41, wherein the conductive bond contacts only the leads.

49. The stacked device of claim 41, wherein the conductive bond has a substantially spherical shape.

50. The stacked device of claim 41, wherein the stacked device is devoid of wire bonds and TAB leads.

51. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly, extends laterally from the first peripheral side surface a first distance, extends downwardly beyond the first bottom surface, does not overlap any insulative material of the first device and is not overlapped by any insulative material of the first device;

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat, extends laterally from the second peripheral side surface a second distance, does not extend downwardly beyond the second bottom surface, does not overlap any insulative material of the second device and is not overlapped by any insulative material of the second device; and

a conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device, does not overlap any insulative material of the stacked device, is not overlapped by any insulative material of the stacked device, extends laterally beyond the first peripheral side surface a third distance and contacts and electrically connects the leads;

wherein the insulative housings are essentially identical to and vertically aligned with one another, the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, and the first distance is greater than the second and third distances.

52. The stacked device of claim 51, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

53. The stacked device of claim 51, wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

54. The stacked device of claim 51, wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral

side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

55. The stacked device of claim 54, wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

56. The stacked device of claim 51, wherein the conductive bond is laterally aligned with the second bottom surface, and is not laterally aligned with the first bottom surface.

57. The stacked device of claim 51, wherein the conductive bond does not contact any insulative material of the stacked device.

58. The stacked device of claim 51, wherein the conductive bond contacts only the leads.

59. The stacked device of claim 51, wherein the conductive bond has a substantially spherical shape.

60. The stacked device of claim 51, wherein the stacked device is devoid of wire bonds and TAB leads.

61. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly;

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat;

a third semiconductor package device, comprising:

a third insulative housing with a third top surface, a third bottom surface, and a third peripheral side surface between the third top and bottom surfaces;

a third semiconductor chip within the third insulative housing, wherein the third chip includes a third upper surface and a third lower surface, and the third upper surface includes a third conductive pad; and

a third lead that protrudes laterally from and extends through the third peripheral side surface and is electrically connected to the third pad, wherein the third lead outside the third insulative housing is flat;

a first conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device and contacts and electrically connects the first and second leads; and

a second conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device and contacts and electrically connects the second and third leads;

wherein the third insulative housing overlaps the second insulative housing, the second insulative housing overlaps the first insulative housing, the third lead overlaps the second lead outside the insulative housings, the second lead overlaps the first lead outside the insulative

housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, and the second top surface faces towards the third bottom surface.

62. The stacked device of claim 61, wherein the first upper surface faces towards the first bottom surface, the second upper surface faces towards the second bottom surface, and the third upper surface faces towards the third bottom surface.

63. The stacked device of claim 61, wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing, and the third lead does not extend downwardly beyond the third bottom surface outside the third insulative housing.

64. The stacked device of claim 61, wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, the third lead extends laterally from the third peripheral side surface a third distance, and the first distance is greater than the second and third distances.

65. The stacked device of claim 61, wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

66. The stacked device of claim 65, wherein the second lead outside the second insulative housing and the third lead outside the third insulative housing are essentially identical to the inner lateral portion of the first lead.

67. The stacked device of claim 61, wherein the conductive bonds are spaced from the insulative housings.

68. The stacked device of claim 61, wherein the conductive bonds are outside the peripheries of the insulative housings.

69. The stacked device of claim 61, wherein the conductive bonds have substantially spherical shapes.

70. The stacked device of claim 61, wherein the stacked device is devoid of wire bonds and TAB leads.

71. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces, wherein the first bottom surface includes a peripheral ledge and a central portion that is within and recessed relative to the peripheral ledge, and the peripheral ledge and the central portion form a cavity;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad;

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly; and

a first terminal that extends through the central portion, is spaced from the first peripheral side surface, is spaced and separated from the first lead outside the first insulative housing and is electrically connected to the first lead and the first pad inside the first insulative housing; and

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat;

a third semiconductor package device, comprising:

a third insulative housing;

a third semiconductor chip within the third insulative housing, wherein the third chip includes a third upper surface and a third lower surface, and the third upper surface includes a third conductive pad; and

a third terminal that extends through the third insulative housing and is electrically connected to the third pad;

a first conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device and contacts and electrically connects the leads; and

a second conductive bond inside the cavity that contacts and electrically connects the terminals;

wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, the first terminal overlaps the third terminal, and the third device extends into the cavity and does not extend outside a periphery of the cavity.

72. The stacked device of claim 71, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

73. The stacked device of claim 71, wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.

74. The stacked device of claim 71, wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

75. The stacked device of claim 71, wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

76. The stacked device of claim 75, wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

77. The stacked device of claim 71, wherein the first conductive bond is spaced from the insulative housings.

78. The stacked device of claim 71, wherein the first conductive bond is outside the peripheries of the insulative housings.

79. The stacked device of claim 71, wherein the first conductive bond has a substantially spherical shape.

80. The stacked device of claim 71, wherein the stacked device is devoid of wire bonds and TAB leads.

81. A three-dimensional stacked semiconductor package device, comprising:

a first semiconductor package device, comprising:

a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces;

a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and

a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly;

a second semiconductor package device, comprising:

a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces, wherein the second bottom surface includes a peripheral ledge and a central portion that is within and recessed relative to the peripheral ledge, and the peripheral ledge and the central portion form a cavity;

a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad;

a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat; and

a second terminal that extends through the central portion, is spaced from the second peripheral side surface, is spaced and separated from the second lead outside the second insulative housing and is electrically connected to the second lead and the second pad inside the second insulative housing;

a third semiconductor package device, comprising:

a third insulative housing;

a third semiconductor chip within the third insulative housing, wherein the third chip includes a third upper surface and a third lower surface, and the third upper surface includes a third conductive pad; and

a third terminal that extends through the third insulative housing and is electrically connected to the third pad;

a first conductive bond outside the insulative housings that extends laterally beyond any insulative material of the stacked device and contacts and electrically connects the leads; and

a second conductive bond inside the cavity that contacts and electrically connects the terminals;

wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, the second terminal overlaps the third terminal, and the third device extends into the cavity and does not extend outside a periphery of the cavity.

82. The stacked device of claim 81, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

83. The stacked device of claim 81, wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.

84. The stacked device of claim 81, wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

85. The stacked device of claim 81, wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that

extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

86. The stacked device of claim 85, wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

87. The stacked device of claim 81, wherein the first conductive bond is spaced from the insulative housings.

88. The stacked device of claim 81, wherein the first conductive bond is outside the peripheries of the insulative housings.

89. The stacked device of claim 81, wherein the first conductive bond has a substantially spherical shape.

90. The stacked device of claim 81, wherein the stacked device is devoid of wire bonds and TAB leads.

91. A method of making a three-dimensional stacked semiconductor package device, comprising:

providing a first semiconductor package device that includes a first insulative housing, a first semiconductor chip and a first lead, wherein the first insulative housing includes a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces, the first chip is within the first insulative housing, the first chip includes a first upper surface and a first lower surface, the first upper surface includes a first conductive pad, and the first lead protrudes laterally from and extends through the first peripheral side surface, is electrically connected to the first pad and is flat outside the first insulative housing;

providing a second semiconductor package device that includes a second insulative housing, a second semiconductor chip and a second lead, wherein the second insulative housing includes a second top surface, a second bottom surface, and a second peripheral side surface

between the second top and bottom surfaces, the second chip is within the second insulative housing, the second chip includes a second upper surface and a second lower surface, the second upper surface includes a second conductive pad, and the second lead protrudes laterally from and extends through the second peripheral side surface, is electrically connected to the second pad and is flat outside the second insulative housing;

bending the first lead downwardly outside the first insulative housing; then

positioning the first and second devices so that the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface; and

electrically connecting the leads using a conductive bond that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts the leads outside the insulative housings, wherein the first lead remains bent and the second lead remains flat outside the insulative housings.

92. The method of claim 91, wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

93. The method of claim 91, wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.

94. The method of claim 91, wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

95. The method of claim 91, wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends

laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

96. The method of claim 95, wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

97. The method of claim 91, wherein the conductive bond is spaced from the insulative housings.

98. The method of claim 91, wherein the conductive bond is outside the peripheries of the insulative housings.

99. The method of claim 91, wherein the conductive bond has a substantially spherical shape.

100. The method of claim 91, wherein the stacked device is devoid of wire bonds and TAB leads.